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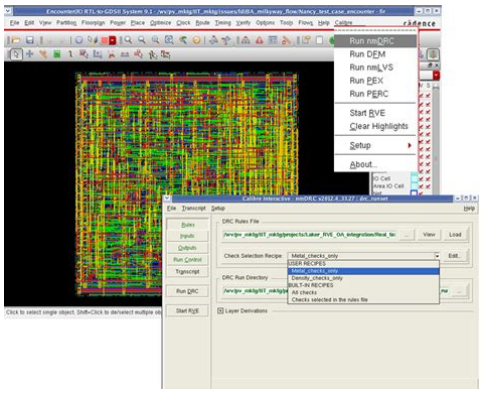

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Book Descriptions:

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Cadence Opus environment using the Alliance cell libraries. This courseCAD for VLSI of the University of Pierre et Marie Curie of Paris. TheDuring the first year this courseVLSI developed at the laboratory and distributed freely all around theThe design kit allows one to designDuring the course the studentsMicro Devices company starting from its architecture specification. InDownload fulltext PDF This work resulted in a design kit for the Alliance libraries. The design steps supported by the design kit up to no w we still develop other issues like HDL synthesis etc. are presented in the following subsections. 2.1. Alliance layout Importation and Exportation In order to be able to use the Cadence Opus tools using the cells and blocks created under the Alliance environment we wrote SKILL programming language under Cadence Opus functions that permit the importation and exportation of symbolic layout from or to the Alliance physical format. These two functions take care of the adequation of the two types of information in the two different environments Cadence and Alliance. The functions are executed either as command lines or menu driven operations. 2.2. Creating a new cell in Cadence Opus using the Alliance libraries To create a new cell we need three different cellviews schematic representing the schematic at the transistor level of the cell layout composed of the different masks used in its fabrication symbol representing a comprehensive view of the cells that will be used hierarchically to build larger designs 2.3. Design rule checking DRC In order to test the layouts of the new cells and the routed views of the designs we wrote a DRC technology file.For example to place and route a design we need two different views a symbol view of the cells to create a schematic to be placed and routed an abstract view of the cells. This view is a reduced description of the physical attributes of the cell.http://www.rh-arch.com/content/file/dewalt-xrp-dc925-manual.xml

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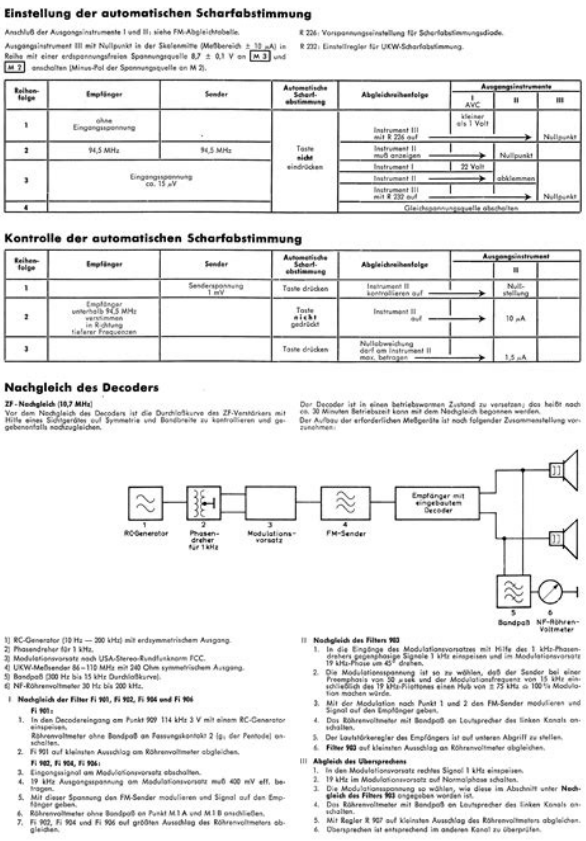
Relying on these view we parametrized the Placement and Routing tools of Cadence Opus. We tested this by creating small designs. The Abstract view is created automatically from the layout of the cells. The function permitting this has also been parametrized. The only indication to give to Cadence Opus in order to do this then is the type of the cell standard cell, pad, jumper, corner,.. The symbol view is created manually under the symbol design tool of Opus. This step is believed to be very important in the design process and is fully supported by the design kit. 2.7. Functional Simulation and Timing Analysis The functional Verilog simulator and the Timing Analysis tools have been parametrized. A Verilog description for each cell in the Alliance library has been written and contains all the information necessary to simulate the designs. The timing analysis tool has been parametrized to allow the computation of delays in a circuit designed using the Alliance cells libraries. 3. General plan of the course The main aim of this course is to teach the students the use of a commercial set of CAD tools for VLSI to design complete circuits. The students got the extra knowledge of how to parametrize a cells library for use under the Cadence Opus environment. This course allowed the students to design complete circuits of average complexity under Cadence Opus. Moreover the students were introduced to the concepts of parametrizing cells libraries for use under the Cadence Opus environment. Actually, the Alliance cells libraries standard cells, pads are fully parametrized for a complete and efficient use under the Cadence Opus environment. Alliance is a set of complete CAD tools and portable libraries for VLSI available for free. Large circuits have been fully designed under Alliance and then successfully fabricated. The design kit is also available for free.http://atomleasing.ru/media/dewalt_tools_owners_manuals.xml

ALLIANCE A complete Set of CAD Tools for teaching VLSI Design Article Sep 1997 Alain Greiner Franois Pcheux The ALLIANCE package is a complete set of CAD tools for teaching VLSI design. ALLIANCE aims at allowing universities to start and develop VLSI design activities without too much time and money investments. Each ALLIANCE tool can operate as a standalone program as well as a part of the complete design framework. The basic design flow is first presented, then each tool is reviewed. Experience and results conclude the paper. 1. Introduction The ALLIANCE package is the result of ten years effort spent at the MASI Laboratory of the Pierre et Marie Curie University UPMC, in Paris. During these years, our major goal was to provide our undergraduate and graduate students with a complete CAD framework, designed to assist them in VLSI CMOS course. The CAOVLSI team focuses its activity on two key issues parallel architectures using high complexity ASICs, and innovative CAD tools for VLSI design. Strong interaction exists between the Hardware Architecture team 15 PHD students and 6 per. Ideas behind the mazerunning algorithm and the hierarchical routing algorithm are combined into a powerful algorithm called hybrid routing. Hybrid routing is based on the mazerunning method with a third search dimension added. The extra search space is built by recursively constructing a hierarchy of coarser grid meshes. By means of a parametercontrolled expansion into the coarser meshes, the hybrid router is able to find the preferred search region very quickly and will not miss local information as a hierarchical router does. For the first time our study reveals the gap between the results produced by these tools versus true optimal solutions. The wirelengths produced by these tools are 1.59 to 2.40 times the optimal in the worst cases, and are 1.43 to 2.12 times the optimal on average.

As for scalability, the average solution quality of each tool deteriorates by an additional 9% to 17% when the problem size increases by a factor of ten. These results indicate significant room for improvement in existing placement algorithms. 3 We studied the impact of nonlocal nets on the quality of the placers by extending the PEKO algorithm PEKU algorithm to generate synthetic placement benchmarks with a known upper bound of the optimal wirelength. For these benchmarks, the wirelengths produced by these tools are 1.75 to 2.18 times the wirelength upper bound in the Moreover, in our study we found that the effectiveness of the algorithms varies for circuits with different characteristics.First, issues on interconnectSecond, issues related to librarygenerating tools, which includeFinally we discuss our approach in DRAMRIS BibTeX Plain Text What do you want to download. Citation only Citation and abstract Download ResearchGate iOS App Get it from the App Store now. Install Keep up with your stats and more Access scientific knowledge from anywhere or Discover by subject area Recruit researchers Join for free Login Email Tip Most researchers use their institutional email address as their ResearchGate login Password Forgot password. Keep me logged in Log in or Continue with LinkedIn Continue with Google Welcome back. Keep me logged in Log in or Continue with LinkedIn Continue with Google No account. All rights reserved. Terms Privacy Copyright Imprint. To browse Academia.edu and the wider internet faster and more securely, please take a few seconds to upgrade your browser. You can download the paper by clicking the button above.



Einstellung der automatischen Scharfabstimmung

Anschluß der Ausgangsinstrumente I und II; siehe FM-Abgleichtabelle.

Ausgangsinstrument III mit Nullpunkt in der Skalenmitte (Meßbereich ± 10 µA) in Reihe mit einer entspannungsfreien Spannungsquelle 8,7 ± 0,1 V an M 3 und M 7 anschalten (Minus-Pol der Spannungsquelle an M 2).

R 226: Vorspannungseinstellung für Scharfabstimmungsdiode.

R 232: Einstellregler für UKW-Scharfabstimmung.

Reihenfolge	Empfänger	Sender	Automatische Scharfabstimmung	Abgleichreihenfolge	Ausgangsinstrumente I AVC	II	III
1	ohne Eingangsspannung		Taste nicht eindrücken	Instrument III mit R 226 auf	kleiner als 1 Volt	→	Nullpunkt
2	94,5 MHz	94,5 MHz		Instrument II muß anzeigen		→ Nullpunkt	
3	Eingangsspannung ca. 15 µV			Instrument I	22 Volt		
				Instrument II		→ abklemmen	
4				Instrument III mit R 232 auf		→	Nullpunkt
				Gleichspannungsquelle abschalten			

Kontrolle der automatischen Scharfabstimmung

Reihenfolge	Empfänger	Sender	Automatische Scharfabstimmung	Abgleichreihenfolge	Ausgangsinstrument II	III
1		Senderspannung 1 mV	Taste drücken	Instrument III kontrollieren auf	→	Nullstellung
2	Empfänger unterhalb 94,5 MHz verstimmen in Richtung tieferer Frequenzen		Taste nicht gedrückt	Instrument II auf	→	10 µA
3			Taste drücken	Nullabweichung darf am Instrument II max. betragen	→	1,5 µA

Nachgleich des Decoders

ZF - Nachgleich (10,7 MHz)

Vor dem Nachgleich des Decoders ist die Durchlaßkurve des ZF-Verstärkers mit Hilfe eines Sichtgerätes auf Symetrie und Bandbreite zu kontrollieren und gegebenenfalls nachzugleichen.

Der Decoder ist in einen betriebswarmen Zustand zu versetzen; das heißt nach ca. 30 Minuten Betriebszeit kann mit dem Nachgleich begonnen werden.

Der Aufbau der erforderlichen Meßgeräte ist nach folgender Zusammenstellung vorzunehmen:

1) RC-Generator (10 Hz — 200 kHz) mit erdsymmetrischem Ausgang.
2) Phasendreher für 1 kHz.
3) Modulationsvorsatz nach USA-Stereo-Rundfunknorm FCC.
4) UKW-Meßsender 86 – 110 MHz mit 240 Ohm symmetrischem Ausgang.
5) Bandpaß (300 Hz bis 15 kHz Durchlaßkurve).
6) NF-Röhrenvoltmeter 30 Hz bis 200 kHz.

I **Nachgleich der Filter Fi 901, Fi 902, Fi 904 und Fi 906**

Fi 901:

1. In den Decodereingang am Punkt 909 114 kHz 3 V mit einem RC-Generator einspeisen. Röhrenvoltmeter ohne Bandpaß an Fassungskontakt 2 (g₂ der Pentode) anschalten.
2. Fi 901 auf kleinsten Ausschlag am Röhrenvoltmeter abgleichen.

Fi 902, Fi 904, Fi 906:

3. Eingangssignal am Modulationsvorsatz abschalten.
4. 19 kHz Ausgangsspannung am Modulationsvorsatz muß 400 mV eff. betragen.
5. Mit dieser Spannung den FM-Sender modulieren und Signal auf den Empfänger geben.
6. Röhrenvoltmeter ohne Bandpaß an Punkt M 1 A und M 1 B anschließen.
7. Fi 902, Fi 904 und Fi 906 auf größten Ausschlag des Röhrenvoltmeters abgleichen.

II **Nachgleich des Filters 903**

1. In die Eingänge des Modulationsvorsatzes mit Hilfe des 1 kHz-Phasendrehers gegenphasige Signale 1 kHz einspeisen und im Modulationsvorsatz 19 kHz-Phase um 45° drehen.
2. Die Modulationsspannung ist so zu wählen, daß der Sender bei einer Preemphasis von 50 µsek und der Modulationsfrequenz von 15 kHz einschließlich des 19 kHz-Pilottones einen Hub von ± 75 kHz = 100 % Modulation machen würde.
3. Mit der Modulation nach Punkt 1 und 2 den FM-Sender modulieren und Signal auf den Empfänger geben.
4. Das Röhrenvoltmeter mit Bandpaß an Lautsprecher des linken Kanals anschalten.
5. Der Lautstärkeregler des Empfängers ist auf unteren Abgriff zu stellen.
6. **Filter 903** auf kleinsten Ausschlag am Röhrenvoltmeter abgleichen.

III **Abgleich des Übersprechens**

1. In den Modulationsvorsatz rechtes Signal 1 kHz einspeisen.
2. 19 kHz im Modulationsvorsatz auf Normalphase schalten.
3. Die Modulationsspannung so wählen, wie diese im Abschnitt unter **Nachgleich des Filters 903** eingegeben worden ist.
4. Das Röhrenvoltmeter mit Bandpaß an Lautsprecher des linken Kanals anschalten.
5. Mit Regler R 907 auf kleinsten Ausschlag des Röhrenvoltmeters abgleichen.
6. Übersprechen ist entsprechend im anderen Kanal zu überprüfen.

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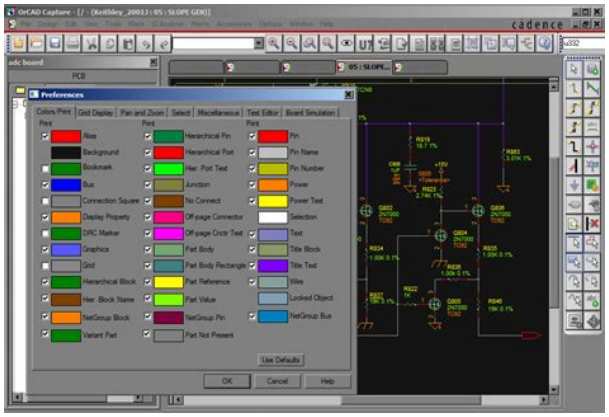

It is capable of modifying circuit, Consequently Therefore they apply to all analyses Otherwise all The object is located within outerHierarchy a list of instances with If outerHierarchy is not given Because SPICE OPUS treats the hierarchical paths of all objects in the The available Colon is used as the separator between So m1x1x2 is an instance named m1 If what is a list of strings a multiple save directives are returned Because SPECTRE knows no such thing as vector parameters, index The name of the parameter can be specified with If parameter is temperature a sweep of the Otherwise the parameters are passed If it is not given If debug is above 2 full simulator output is printed. Setting it to If gain is given as This does not mean that any results were produced. It only means that the return code from the simuator was 0 OK. Finally the Its return value is stored in the If there are n jobs in the job list. This means we have n job groups with one job per job group. Integer, real, and string simulator options are converted with the All parameters It is written to. The group recruits and places all types of engineering, technical and manufacturing professionals using SPI’s extensive, prescreened database of consultants. Qualified talent includes You can learn more about our use of cookies and configure your browser settings in order to avoid cookies by clicking our cookie policy. By navigating the website, you agree to our use of cookies. This means taking into account not just the chips in the system, but also the packages, boards, and the software load that. I am looking for a copy of advanced Skill manual for either edge or opus or both. International Cadence User Group this summer in August. This tutorial. Cadence Skill Reference Manual Contents. History SKILL was originally based on a flavor of Lisp called “” created at by the students of Professor. SKILL is not an acronym; it is a name. For trademark reasons Cadence prefers it be capitalized.

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And all other flavors of were eventually superseded by an standard for Lisp called . Historically, SKILL was known as IL. SKILL was a library of IL functions. The name was originally an initialism for Silicon Compiler Interface Language SCIL, pronounced SKIL, which then morphed into SKILL, a plain English word that was easier for everyone to remember. IL was just Interface Language. Whilst SKILL was used initially to describe the rather than the language, the snappier name stuck. The name IL remains a common file extension used for code .il designating that the code contained in the file has lisp2 semantics. Another possible file extension is .ils designating that the content has lisp1 semantics. Traditional syntax such as car mylist can be mixed with such as carmylist White space between the function name and the opening parenthesis, as in car mylist is also allowed but has a different meaning. For example, list car mylist or equivalently listcar mylist has the traditional lisp meaning of a call to the list function with two operands car and mylist, the first of which is a variable reference, and the second a call to the mylist function. Usually this is not what the beginner programmer intended. Thus, SKILL novices usually incorrectly think of car mylist as a syntax error. Certain arithmetic operations can be also called using an. SKILL indeed internally represents the language as traditional Lisp, the surface syntax loosens this restriction compared to other lisps. More elaborate examples look quite different from their Lisp equivalents. For example, the factorial function in SKILL may be represented several different ways which are all compiled to the identical internal representation. A SKILL is currently hosted on under the name skillschool link. Cadence Skill Reference Manual Cadence also hosts two SKILL users group forums on their website. One is dedicated to Allegro PCB SKILL PCB SKILL, and the other is dedicated to SKILL Custom IC SKILL.

No known users group currently exists for Cadence Concept SKILL scripting as of May 2010. Watch this fun video. And with large, thumbfriendly keys, errant texts Printed Braille and digital ASCII text phone user.

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